application by the amendments made to the claims, specification or otherwise in the application. For at least the following reasons it is submitted that this application is in condition for allowance. Reconsideration is respectfully requested.

Discussion of Office Action Rejections

Objection to Specification

Regarding to the objection of the disclosure page 2, line 4 of the specification, applicant respectfully responds that the verb used in the sentence ' A plurality of mounting pads 104 being formed on the exterior surface of the laminating board 100 **is** acted as connecting point between the laminating board 100 and the chip 110.' is correct. The verb ' **is**' is used instead of ' are' because the term ' a plurality of mounting pads 104' indicates that a lot of the same type/ kind of mounting pads 104 are provided. If a verb ' are' is used, for example ' a plurality of mounting pads 104 are .....' then the sentence indicates that there are various types of mounting pads 104 (not only plural but different types as well) are provided.

Applicant respectfully requests to withdraw the objection.

Rejection under 35 USC 103 (a)

Claims 1, 5-7 and 11-13 are rejected under 35 USC 103 (a) as being unpatentable over Lach et al. (U. S. Patent No. 6,108,212).

Applicant respectfully traverses this rejection and submits that the cited reference cannot achieve the present invention.

The present invention provides a flip-chip package comprising a plurality of patterned

circuit layers 208, 210, wherein the patterned circuit layers are electrically connected to each other. A solder mask layer 222 covers the patterned circuit layers. The solder mask layer 222 exposes only a portion of the surface 214a and covers the side of the first mounting pad 214 in the peripheral region 218. While for the central region 220, the solder mask layer 222 exposes the surface 216a and side surfaces 216b completely to form a pad opening 224. Therefore, the pitch 230 of the first mounting pads 214 is smaller than the pitch 232 of the second mounting pads 216.

Lach et al discloses a SMD package wherein the chip 12 is attached onto the conductor 22 by solders 64; however, the first mounting pad 27 is formed below the interposer 14 (Fig. 1). The first mounting pad 27 is connected to a substrate 18 by the solder bump 28. It is obvious that the mounting pads 26, 27 are not used for connecting the chip 12 to the substrate 18 directly. Instead, the mounting pads 26 and 27 are used for connecting the interposer 14 to the substrate 18.

Although Lach et al discloses using the completely exposed mounting pad 26 and the partly exposed mounting pad 27. However, the mounting pads 26 or 27 are not used for directly connecting the chip to the substrate because the mounting pads of Lach are formed underneath of the interposer 14 for connecting the interposer 14 to the substrate 18. Applicant would like to particularly point the mounting pads of the present invention are formed with the combination of the SMD and NSMD designs so that the bonding problem of solder bumps between the chip and the substrate can be resolved. Further, the arrangement of the partly exposed first mounting pads 214 at the peripheral region 218 and the completely exposed second mounting pads 216 at the central region 220 of the substrate is according to the area-array arrangement of the chip/chips to the substrate. Such teaching is neither disclosed nor recognized by Lach et al.

Since Lach dose not disclose forming the completely exposed mounting pad 26 and the

partly exposed mounting pad 27 on the substrate 18 for directly bonding the chip to the substrate. Neither dose Lach disclose specifically that the mounting pads 26 are disposed on the central region and mounting pads 27 are disposed on the peripheral region. Further, Lach dose not disclose, suggest or hint to combine the SMD and NSMD designs together to form the mounting pads in order to resolve the solder bumps problems. Therefore, applicant respectfully submits that it is improper for the Office Action to interpret that the mounting pads 27 of Lach are disposed on the peripheral region of the substrate and the mounting pads 26 of Lach are disposed on the central region of the substrate.

Further, applicant respectfully disagrees with the Office Action that the design of the mounting pads in Lach is the same as the present invention because a Non Solder Mask Define (NSMD) mounting pad dose not mean there is no solder mask at all. Instead, the solder mask is designed in such a way that solder mask formed on the mounting pad has an opening to expose the side surfaces and top surface of the mounting pad. The present invention, as recited in claims 1 and 7, teaches a solder mask layer to cover the entire patterned circuit layer such that only a portion of the top surface of the first mounting pad that is on the patterned circuit layer is exposed, while the whole top surface of the second mounting pad that is on the patterned circuit layer is exposed. In other words, the solder mask layer is covering both the side surface and a part of the top surface of the first mounting pad. Moreover, the solder mask layer is also present around the area of the second mounting pad.

However, it is obvious from Figs 1 and 10 and from Column 5, lines 34-38 of Lach that the solder mask 42 is formed on and covered only the resistive material 36 at the portion 2 of the package. The resistive material 36 that is formed on and in-between the component pad 27 and the terminal 34 is to conduct DC between the component pad and the terminal, and therefore can

not be construed as a solder mask layer. It is also clear that around the area of solder pad 26 at the first surface 52, there is no formation of solder mask 42. Since there is no formation of the solder mask 42 or the pad opening, the attached area between the mounting pad 26 and solder bump 28 and the height of the bumps 28 cannot be controlled as recited in present invention.

Furthermore, Lach discloses using design of the SMD package only (Column 3, line 20). Lach dose not disclose, suggest or hint to combine the SMD and NSMD designs together to resolve the solder bumps problems.

For these reasons, applicant respectfully submits that claims 1 and 7 patentably distinguish over Lach et al., and claims 2-14 depending therefrom. Withdrawal of this rejection is respectfully requested.

Claims 2-4, 8-10 and 14 are rejected under 35 USC 103 (a) as being unpatentable over Lach et al. (U. S. Patent No. 6,108,212) in view of Admitted Prior Art (APA).

As discussed above, Lach teaches away from the present invention by forming the mounting pad below the interposer to connect to the substrate instead of forming the mounting pad on top of the substrate to connect the chip directly. Further, Lach fails to disclose the solder mask exposing only a portion of the top surface of the first mounting pad in the peripheral region while exposing the whole surface of the second mounting pad at the central region of the substrate.

Although, APA discloses the formation of NSMD package in Fig.2, however, APA dose not hint or suggest or teach to combine the SMD and NSMD designs together so that the pitch of the first mounting pads at the peripheral region is smaller than the pitch of the second mounting pads at the central region.

Therefore, even if Lach is combined with APA, Applicant respectfully submits that the

combination still fail to achieve the present invention as both fail to disclose the requisite features as recited in amended claims 1 and 7. Reconsideration is respectfully requested.

Claims 4 and 10 are rejected under 35 USC 103 (a) as being unpatentable over Lach et al. (U. S. Patent No. 6,108,212) in view of Admitted Prior Art (APA) and further in view of Katchmar (U. S. Patent No. 6,194,782).

Karchmar discloses a method by arranging more solder bumps 40/ mounting pads 35 at the central region than at the peripheral region of the package shown in Figs. 5 and 6. Therefore applicant respectfully submits that the pitch of the mounting pad 34 at the central region is smaller than the pitch of the mounting pad at the peripheral region, and it is more spacious at the peripheral region of the package (Fig. 5). Therefore, Karchmar teaches away from the present invention by increase the pitch of the mounting pad at the peripheral region instead at the central region.

Therefore applicant respectfully submits that the cited references cannot achieve the present invention as they all fails to disclose the requisite features of the invention. Withdrawal of this rejection is respectfully requested.

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-5 and 7-14 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned. Respectfully submitted.

Respectfully submitted,

Date: November 1, 2001

Belinda Lee
Registration No. 46,863

J.C. Patents
4 Venture, Suite 250
Irvine, CA 92618
Tel.: (949) 660-0761

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claim

Please amend claims 1, 7 and 12 as follows and please delete claim 6:

1. (Once Amended) A substrate structure of Flip Chip package comprising:

a plurality of patterned circuit layer;

at least an insulative layer stacked between the patterned circuit layers for isolating the patterned circuit layers, and the patterned circuit layers are electrically connected one another, and one of the patterned circuit layer is positioned on the surface of the substrate of the flip chip package, and the patterned circuit layer comprises at least a plurality of a first mounting pad and a plurality of a second mounting pad; and

a solder mask layer covering the patterned circuit layer on the surface of the substrate of the flip chip package, [and] a portion of the surface on the outer edge of the first mounting pad and a side surface of the first mounting pad while exposing a portion of the surface of the first mounting pad and the whole surface of the second mounting pad, wherein the first mounting pads are disposed on the peripheral region of the substrate and the second mounting pads are disposed at a central region of the substrate.

7. (Once Amended) A substrate structure of Flip Chip package comprising:

a plurality of patterned circuit layer;

at least an insulative layer stacked between the patterned circuit layers for isolating the patterned circuit layers, and the patterned circuit layers are electrically connected one another, and one of the patterned circuit layer is positioned on the surface of the substrate of

the flip chip package, and the patterned circuit layer comprises at least a plurality of a first mounting pad and a plurality of a second mounting pad;

a solder mask layer covering the patterned circuit layer on the surface of the substrate of the flip chip package and a portion of the surface on the outer edge of the first mounting pad while exposing a portion of the surface of the first mounting pad and the whole surface of the second mounting pad, wherein the first mounting pads are formed at the peripheral region of the substrate;

a chip having an active surface with a plurality of bumps disposed thereon wherein the chip has its active surface face to the surface of the substrate of the flip chip package, and the bumps are electrically connected to their corresponding first bonding pads and second bonding pads respectively; and

an underfill material filling between the active surface of the chip and the top surface of the substrate of the flip chip package.

12. (Once Amended) The substrate structure of Flip Chip package of claim 7 wherein [the first mounting pads are disposed in the peripheral region of the substrate of the flip chip package while] the second mounting pads are disposed in the central region of the substrate of the flip chip package.